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33. (New) The memory device of claim 31, wherein said suspend signal represents a byte write suspend command.

1 34. (New) The memory device of claim 31, wherein said control circuit is

2 configured to receive a status request signal and said register is configured to

3 output said status signal in response to said status request signal, said status

signal having a first state to indicate said write operation is suspended and a

second state tp indicate said write operation is not suspended.

35. (New) The memory device of claim 35, further comprising:

at least one data input/output coupled to said control circuit, wherein the at

least one data input/output is configured to receive said status request signal

4 from a processor and to provide said status signal to said processor.

1 36. (New) The memory device of claim 31, further comprising:

2 a status output coupled to said register, wherein said status output is

3 configured to provide a second status signal when said status output is polled,

4 and wherein said second status signal having a first state to indicate said write

operation is suspended and a second state to indicate said write operation is not

6 suspended.

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(New) The memory device of claim 31, wherein said status request signal

2 is a read status register command.